MIRACLE EDUCATIONAL SOCIETY GROUP OF INSTITUTIONS

(AUTONOMOUS)

(*Approved by AICTE NEW DELHI, Accredited by NAAC & Permanently Affiliated to JNTU-GV)*

Miracle City, Bhogapuram, Vizianagaram – 535216

DEPARTMENT
OF
ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech
In
VLSI & EMBEDDED SYSTEMS (Course Code: 68)

R25 REGULATION

BOS APPROVED COURSE STRUCTURE & SYLLABUS

Dt: 07-01-2026

Minutes of the 1st Board of Studies (BOS) Meeting held on 07.01.2026

S.NO	NAME OF THE MEMBER	DESIGNATION	SIGNATURE
1	Dr.B.Nalini , Assistant Professor & HOD ECE, JNTUGV	University Nominee	
2	Dr.M.Jayamanmadha Rao, Professor, AITAM , Tekkali	Subject Expert	
3	Dr.G.Anantha Rao, Associate Professor, AVEV, VZM	Subject Expert	
4	Dr.M.Satya Prasad, DGM, BSNL, Visakhapatnam	Industry Expert	
5	Smt. K. Bhavani, Miracle software systems	Alumni	
6	Dr.T.Ravibabu	Internal Member	
7	Dr.A.Venkateswara Rao	Internal Member	
8	Mr.N.Seshu Kumar	Internal Member	
9	Mrs.P.Sridevi	Internal Member	
10	T Narasimha Murthy	Internal Member	
11	Mrs.P.Sailaja	Internal Member	
12	Mr.Ch.Subbarao	Internal Member	
13	S.Devendra	Internal Member	
14	A Ganesh	Internal Member	
15	Nansi Neitngale Thote	Internal Member	
16	Mrs.D.Rajitha, HOD	BOS Chairman	

2nd Board of Studies Meeting

The Board of Studies Meeting of Department of Electronics and Communication Engineering was convened at 12:30 P.M. on 07-01-2026 (Thursday) through online (Zoom Meeting) mode under the chairmanship of Mrs.D.Rajitha, Head of the Department.

Agenda:

Welcoming the distinguished members of the Board of studies meeting by the HOD

1. Discussion about Course Structure of the III & IV B.Tech Program R23.
2. Discussion about Course Structure of the M.Tech Program R25.
3. Discussion about R23 –B.Tech – III year I and II Sem Syllabus.
4. Discussion about R23 –B.Tech – IV year I and II Sem Syllabus.
5. Discussion about R23 –M.Tech – I year I and II Sem Syllabus.
6. Discussion about R23 –M.Tech – II year I and II Sem Syllabus.
7. Discussion about the credits in the course structure.
8. Discussion about the methodologies for teaching and evaluation.
9. Discussion about the text books, reference books and web references.

Any other item with the approval of the chair.

Minutes of the meeting:

1. The chairperson of the BoS, Mrs.D.Rajitha, welcomed the committee members to the online meeting conducted on 07-01-2026 via the Google Meet platform at12:30P.M.
2. The chairperson also extended a warm welcome to the internal committee members.
3. The committee reviewed the course structure and syllabi for the B.Tech and M.Tech programs in Electronics and Communication Engineering.
4. The course structure, syllabus for the III year I and II Semester, IV year I and II Semester of R23 B.Tech (ECE), and M.Tech (ECE) - VLSI&ES – 68, including the first and second year semesters and academic regulations, were discussed, reviewed, and approved.
5. The committee examined the credit distribution across the semesters.
6. Discussions were held regarding teaching methodologies, textbooks, and reference materials.
7. **Dr.B.Nalini**, JNTUGV Nominee suggested that the syllabus be revised atleast of 10% from the next batch onward, considering students' ambitions and regional factors.
8. **Dr.M.Jayamanmadha Rao**, Subject Expert, also recommended a syllabus revision from next batch.

7. Dr. R. Rajeswara Rao, the JNTU GV Nominee, suggested that the syllabus be revised by up to 20% from the next batch onward, considering students' ambitions and regional factors.
8. Dr. Ch. Ramesh, Subject Expert, also recommended a syllabus revision of up to 20% starting from the next batch.
9. Dr. B.Kameswara Rao, Subject Expert, also recommended a syllabus revision of up to 10 to 20% starting from the next batch.
10. Dr. S. Sridhar, Professor of CSE, proposed and delivered the vote of thanks at the conclusion of the meeting.

Name of the meeting	**IInd Board of Studies**	**Ref No**	**Email communication dated on 07-01-2026 by the chair Person (BoS)**	**Time**
CSE BOS Meeting	Online Mode (Google Meet)	Date	08-01-2026	03:00 PM
Meeting Link: https://meet.google.com/eho-taui-phn				

Miracle Educational Society Group of Institutions (A)Bhoghapuram-535216
Department of Electronics and Communication Engineering

Academic Regulations of M. Tech (Regular/Full Time) Programmes, 2025-26 (R25)
Under Choice Based Credit System (CBCS) 2025-26 (R25)
(Effective for the students admitted into I Year from the Academic Year 2025-26 and onwards)

1.0 **Post-Graduate Degree Programmes in Engineering & Technology (PGP in E & T) Miracle Educational Society Group Of Institutions** offers **Two** Years (**Four** Semesters) full-time Master of Technology (M.Tech.) Degree programmes, under Choice Based Credit System (CBCS) at its constituent (non-autonomous) and affiliated colleges in different branches of Engineering and Technology with different specializations.

2.0 **Eligibility for Admissions**

2.1 Admission to the PGPs shall be made subject to eligibility, qualification and specializations prescribed by the University from time to time, for each specialization under each M. Tech programme.

2.2 Admission to the post graduate programme shall be made on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by Andhra Pradesh State Government (PGECET) for M. Tech. programmes / an entrance test conducted by JNTU-GV/ on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.3 The medium of instructions for all PG Programmes will be **ENGLISH** only.

3.0 **M. Tech. Programme (PGP in E & T) Structure**

3.1 The M. Tech. Programs in E & T of JNTU-GV are of Semester pattern, with **Four** Semesters consisting of **Two** academic years, each academic year having **Two** Semesters (First/Odd and Second/Even Semesters). Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per Semester.

3.2 The two-year M. Tech. program consists of **80** credits and the student has to register for all **80** credits and earn all **68** credits for the award of M. Tech. degree. There is **NO** exemption of credits in any case.

3.3 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M. Tech. degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M. Tech. programme.

3.4 **UGC/AICTE** specified definitions/descriptions are adopted appropriately for various terms and abbreviations used in these PG academic regulations, as listed below:

3.4.1 **Semester Scheme**

Each Semester shall have 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) are taken as 'references' for the present set of Regulations. The terms 'SUBJECT' and 'COURSE' imply the same meaning here and refer to 'Theory Subject', or 'Lab Course', or 'Design/Drawing Subject', or 'Mini Project with Seminar', or 'Dissertation', as the case may be.

3.4.2 Credit Courses

All subjects/courses are to be registered by the student in a semester to earn credits which shall be assigned to each subject/course in an L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods: Credits) structure based on the following general pattern: One credit for one hour/week/semester for theory/lecture (L) courses

- One credit for two hours/ week/semester for laboratory/ practical (P) courses or tutorials (T)

Other student activities like study tour, guest lecture, conference/workshop participations, technical paper presentations and mandatory courses (***Non-credit Audit Courses***) will not carry any credits.

3.4.3 Subject Course Classification

All subjects/courses offered for the Post-Graduate Programme in E & T (M. Tech. Degree Programme) are broadly classified as follows. The College has followed in general the guidelines issued by AICTE/UGC.

S. No.	Broad Course Classification	Course Group/ Category	Course Description
1	Core Courses (CoC)	PC- Professional Core	Includes subjects related to the parent discipline/department/ branch of Engineering
		Dissertation	M. Tech. Project or PG Project or Major Project
		Mini Project with Seminar	Seminar based on core contents related to Parent Discipline/ Department/ Branch of Engineering
2	Elective Courses (EtE)	PE - Professional Electives	Includes elective subjects related to the parent discipline/department/branch of Engineering
		OE - Open Electives	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline/department/ branch of Engineering
3	***Mandatory Courses***	--	***Non-Credit Audit Courses***

4.0 Course Registration

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each specialization, who will advise on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice/Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.

4.2 The Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work through 'ON-LINE SUBMISSIONS', ensuring 'DATE and TIME Stamping'. The ON-LINE Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply for ON-LINE Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries during ON-LINE Registration for the Subject(s) / Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Subject/ Course in that Category will be taken into

consideration.

4.5 Subject/ Course Options exercised through ON-LINE Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices also will not be considered. However, if the Subject/ Course that has already been listed for Registration by the University in a Semester could not be offered due to unforeseen or unexpected reasons, then the Student will be allowed to have alternate choice either for a new Subject, if it is offered, or for another existing Subject (subject to availability of seats). Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

5.0 Attendance Requirements

The programmes are offered based on a unit system with each subject being considered a unit. Attendance is calculated separately for each subject.

5.1 Attendance in all classes (Lectures/Laboratories) is compulsory. The minimum required attendance in each theory subject (***also mandatory Audit Courses***) including the attendance of mid-term examination / Laboratory etc. is 75%. Two periods of attendance for each theory subject shall be considered, if the student appears for the mid-term examination of that subject. ***This attendance should also be included in the attendance uploaded every fortnight in the University Website. The attendance of mandatory Audit Courses should be uploaded separately to the University.*** A student shall not be permitted to appear for the Semester End Examinations (SEE), if his attendance is less than 75%.

5.2 A student's Seminar report and presentation on Mini Project shall be eligible for evaluation, only if he ensures a minimum of 75% of his attendance in Seminar presentation classes on Mini Project during that Semester.

5.3 **Condoning of shortage of attendance** (between 65% and 75%) up to a maximum of 10% (considering the days of attendance in sports, games, NCC, NSS activities and Medical grounds) in each subject (Theory/Lab/Mini Project with Seminar) of a semester shall be granted by the College Academic Committee on genuine reasons.

5.4 A prescribed fee per subject shall be payable for condoning shortage of attendance after getting the approval of College Academic Committee for the same. The College Academic Committee shall maintain relevant documents along with the request from the student.

5.5 Shortage of Attendance below 65% in any subject shall in **no case be condoned.**

5.6 A Student, whose shortage of attendance is not condoned in any Subject(s) (Theory/Lab/Mini Project with Seminar) in any Semester, is considered as 'Detained in that Subject(s), and is not eligible to write Semester End Examination(s) of such Subject(s), (in case of Mini Project with Seminar, his/her Mini Project with Seminar Report or Presentation are not eligible for evaluation) in that Semester; and he/she has to seek re-registration for those Subject(s) in subsequent Semesters, and attend the same as and when offered.

5.7 A student fulfills the attendance requirement in the present semester, shall not be eligible for readmission into the same class.

5.8 **a)** A student shall put in a minimum required attendance in at least **three theory subjects (excluding *mandatory (non-credit audit)* course)** in first Year I semester for promotion to first Year II Semester.

b) A student shall put in a minimum required attendance in at least **three theory subjects (excluding *mandatory (non-credit audit)* course)** in first Year II semester for promotion to second Year I Semester.

6.0 Academic Requirements

The following academic requirements must be satisfied, in addition to the attendance requirements mentioned in item no. 5. The performance of the candidate in each semester shall be evaluated subject- wise, with a maximum of 100 marks per subject / course (theory / practical), based on Internal Evaluation and Semester End Examination.

6.1 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course, if he secures not less than:

- 40% of Marks (24 out of 60 marks) in the Semester End Examination;
- 40% of Marks in the internal examinations (16 out of 40 marks allotted for CIE); and
- A minimum of 50% of marks in the sum total of CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of Letter Grades this implies securing **'B'** Grade or above in a subject.

6.2 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to Mini Project with seminar, if student secures not less than 50% marks (i.e. 50 out of 100 allotted marks). The student would be treated as failed, if student (i) does not submit a seminar report on Mini Project or does not make a presentation of the same before the evaluation committee as per schedule or (ii) secures less than 50% marks in Mini Project with seminar evaluation. The failed student shall reappear for the above evaluation when the notification for supplementary examination is issued.

6.3 A student shall register for all subjects for total of **80** credits as specified and listed in the course structure for the chosen specialization, put in the required attendance and fulfill the academic requirements for securing **80** credits obtaining a minimum of **'B'** Grade or above in each subject, and all **80** credits securing Semester Grade Point Average **(SGPA) ≥ 6.0** (in each semester) and final Cumulative Grade Point Average **(CGPA)** (i.e., CGPA at the end of PGP**) ≥ 6.0**, and shall ***pass all the mandatory Audit Courses*** to complete the PGP successfully.

Note: (1) The SGPA will be computed and printed on the marks memo only if the candidate passes in all the subjects offered and gets minimum B grade in all the subjects.

(2) CGPA is calculated only when the candidate passes in all the subjects offered in all the semesters

6.4 Marks and Letter Grades obtained in all those subjects covering the above specified **80** credits alone shall be considered for the calculation of final CGPA, which will be indicated in the Grade Card /Marks Memo of second year second semester.

6.5 If a student registers for extra subject(s) (in the parent department or other departments/ branches of Engineering) other than those listed subjects totaling to **80** credits as specified in the course structure, the performance in extra subject(s) (although evaluated and graded using the same procedure as that of the required **80** credits) will not be considered while calculating the SGPA and CGPA. For such extra subject(s) registered, percentage of marks and Letter Grade alone will be indicated in the Grade Card/Marks Memo, as a performance measure, subject to completion of the attendance and academic requirements as stated in items 5 and 6.1 - 6.3.

6.6 When a student is detained due to shortage of attendance in any subject(s) in any semester, no Grade allotment will be made for such subject(s). However, he is eligible for re-registration of such subject(s) in the subsequent semester(s), as and when next offered, with the academic regulations of the batch into which he is re-registered, by paying the prescribed fees per subject. In all these re-registration cases, the student shall have to secure a fresh set of internal marks and Semester End Examination marks for

performance evaluation in such subject(s), and SGPA/CGPA calculations.

6.7 A student eligible to appear for the Semester End Examination in any subject, but absent from it or failed (failing to secure 'B' Grade or above), may reappear for that subject at the supplementary examination as and when conducted. In such cases, his Internal Marks assessed earlier for that subject will be carried over, and added to the marks secured in the supplementary examination, for the purpose of evaluating his performance in that subject.

6.8 A Student who fails to earn **80** credits as per the specified course structure, and as indicated above, within **four** academic years from the date of commencement of his first year first semester, shall forfeit his seat in M. Tech. programme and his admission **shall stand cancelled.**

7.0 Evaluation - Distribution and Weightage of Marks

The performance of a student in each semester shall be evaluated subject- wise (irrespective of credits assigned) for a maximum of 100 marks.

7.1 The performance of a student in every subject/course (including practicals and Project) will be evaluated for 100 marks each, with 40 marks allotted for CIE (Continuous Internal Evaluation) and 60 marks for SEE (Semester End-Examination). The Continuous Internal Evaluation shall be made based on the average of the marks secured in the two Mid-Term Examinations conducted, first Mid-Term examinations in the middle of the Semester and second Mid-Term examinations during the last week of instruction.

The descriptive paper shall contain 6 full questions out of which, the student has to answer 3 questions, each carrying 10 marks. The average of the two Mid Term Examinations shall be taken as the final marks for Mid Term Examination (for 30 marks).

The remaining 10 marks of Continuous Internal Assessment (out of 40) are distributed as:

1. Assignment for 5 marks. (Average of 2 Assignments each for 5 marks)
2. Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject for 5 marks.

While the first mid-term examination shall be conducted on 50% of the syllabus, the second mid-term examination shall be conducted on the remaining 50% of the syllabus.

Five (5) marks are allocated for assignments (as specified by the subject teacher concerned). The first assignment should be submitted before the conduct of the first mid-term examination, and the second assignment should be submitted before the conduct of the second mid-term examination. The average of the two assignments shall be taken as the final marks for assignment (for 5 marks).

Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject for 5 marks before II Mid-Term Examination.

- The Student, in each subject, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned subject, if the student scores ≥ 40% (16 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

The details of the end semester question paper pattern are as follows:

7.2 The Semester End Examinations (SEE), for theory subjects, will be conducted for 60 marks consisting of

- Consists of **Six** questions (numbered from 1 to 6) carrying 10 marks each. Each of these questions is from each unit and may contain sub-questions. For each question there will be an "either" "or" choice, which means that there will be two questions from each unit and the student should answer either of the two questions.
- The duration of Semester End Examination is 3 hours.

7.3 For practical subjects there shall be a Continuous Internal Evaluation (CIE) during the semester for 40 marks and 60 marks for semester end examination. Out of the 40 marks for internal evaluation:

1. A write-up on day-to-day experiment in the laboratory (in terms of aim, components/procedure, expected outcome) which shall be evaluated for 10 marks
2. 10 marks for viva-voce (or) tutorial (or) case study (or) application (or) poster presentation of the course concerned.
3. Internal practical examination conducted by the laboratory teacher concerned shall be evaluated for 10 marks.
4. The remaining 10 marks are for Laboratory Project, which consists of the Design (or) Software / Hardware Model Presentation (or) App Development (or) Prototype Presentation submission which shall be evaluated after completion of laboratory course and before semester end practical examination.

The Semester End Examination shall be conducted with an external examiner and the laboratory teacher. The external examiner shall be appointed from the cluster / other colleges which will be decided by the examination branch.

In the Semester End Examination, held for 3 hours, total 60 marks are divided and allocated as shown below:

1. 10 marks for write-up
2. 15 for experiment/program
3. 15 for evaluation of results
4. 10 marks for presentation on another experiment/program in the same laboratory course and
5. 10 marks for viva-voce on concerned laboratory course.

- The Student, in each subject, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned subject, if the student scores ≥ 40% (16 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

7.4 For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Principal of the College and this is to be informed to the Director of Evaluation within two weeks, before commencement of the lab end examinations. The external examiner should be selected from outside the College concerned but within the cluster. No external examiner should be appointed from any other College in the same cluster/any other cluster which is run by the same Management.

7.5 Evaluation Procedure for Seminar:

During the First Semester and Second Semester, the internal evaluation for Seminar–I and Seminar–II shall be conducted for 50 marks each.

Procedure: The Departmental Academic Committee (DAC) will review the progress of the Seminar during the seminar presentations in each semester and evaluate it for 50 marks. The Seminar shall be evaluated by the DAC before the semester-end examinations. The student shall carry out the Seminar in consultation with the mentor, submit the Seminar report to the department, and make an oral presentation before the DAC, which consists of the Head of the Department, the mentor, and two senior faculty members of the department.

7.6 Every candidate shall be required to submit a dissertation on a topic approved by the Dissertation Review Committee.

7.7 A Dissertation Review Committee (DRC) shall be constituted with the Head of the Department as Chairperson, Dissertation Supervisor and one senior faculty member of the Department offering the M.Tech. programme.

7.8 Registration of Dissertation Work: A candidate is permitted to register for the Dissertation Work after satisfying the attendance requirement in all the subjects, both theory and laboratory.

7.9 After satisfying 7.9, a candidate must present in ***Dissertation Work Review - I***, in consultation with his Dissertation Supervisor, the title, objective and plan of action of his Dissertation work to the Dissertation Review Committee (DRC) for approval ***within four weeks*** from the commencement of **Second year First Semester**. Only after obtaining the approval of the DRC can the student initiate the Dissertation work.

7.10 If a candidate wishes to change his supervisor or topic of the Dissertation, he can do so with the approval of the DRC. However, the DRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of Dissertation proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

7.11 A candidate shall submit his Dissertation progress report in two stages at least with a gap of **three** months between them.

7.12 The work on the Dissertation shall be initiated at the beginning of the II year and the duration of the Dissertation is two semesters. A candidate is permitted to submit Dissertation Thesis only after successful completion of all theory and practical courses with the approval of DRC ***not earlier than 40 weeks*** from the date of approval of the Dissertation work. For the approval of DRC, the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the DRC.

7.13 ***The Dissertation Work Review - II*** in II Year I Semester carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and DRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Dissertation Work. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - II. If he fails to obtain the minimum required marks, he has to reappear for Dissertation Work Review - II as and when conducted.

7.14 ***The Dissertation Work Review - III*** in II Year II Sem. carries 100 internal marks. Evaluation should bedone by the DRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The DRC will examine the overall progress of the Dissertation Work and decide whether or not the Dissertation is eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Dissertation Work Review - III as and when conducted. For Dissertation Evaluation (Viva Voce) in II Year II

Semester there are external marks of 100 and it is evaluated by the external examiner.

The candidate has to secure a minimum of 50% marks in Dissertation Evaluation (Viva- Voce) examination.

7.15 Dissertation Work Reviews - II and III shall be conducted in phase I (Regular) and Phase II (Supplementary). Phase II will be conducted only for unsuccessful students in Phase I. The unsuccessful students in Dissertation Work Review - II (Phase II) shall reappear for it at the time of Dissertation Work Review - III (Phase I). These students shall reappear for Dissertation Work Review - III in the next academic year at the time of Dissertation Work Review - II only after completion of Dissertation Work Review - II, and then Dissertation Work Review - III follows. The unsuccessful students in Dissertation Work Review - III (Phase II) shall reappear for Dissertation Work Review - III in the next academic year only at the time of Dissertation Work Review - II (Phase I).

7.16 After approval from the DRC, a soft copy of the thesis should be submitted for ANTI-PLAGIARISM check and the plagiarism report should be submitted to the University and be included in the final thesis. The Thesis will be accepted for submission, if the similarity index is less than **30%**. If the similarity index has more than the required percentage, the student is advised to modify accordingly and re- submit the soft copy of the thesis after one month. The maximum number of re-submissions of thesis after plagiarism check is limited to ***TWO***. The candidate has to register for the Dissertation work and work for two semesters. After three attempts, the admission is liable to be cancelled. The college authorities are advised to make plagiarism check of every soft copy of theses before submissions.

7.17 Three copies of the Dissertation Thesis certified by the supervisor shall be submitted to the College/School/Institute, after submission of a research paper related to the Dissertation work in a UGC approved journal. A copy of the submitted research paper shall be attached to thesis.

7.18 The thesis shall be adjudicated by an external examiner selected by the University. For this, the Principal of the College/School/Institute shall submit a panel of **three** examiners from among the list of experts in the relevant specialization as submitted by the supervisor concerned and Head of the Department.

7.19 If the report of the external examiner is unsatisfactory, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unsatisfactory again, the thesis shall be summarily rejected. Subsequent actions for such dissertations may be considered, only on the specific recommendations of the external examiner and /or Dissertation Review Committee. No further correspondence in this matter will be entertained, if there is no specific recommendation for resubmission.

7.20 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and decide for the conduct of Dissertation Viva-Voce examination. The Dissertation Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis. The candidate has to secure a minimum of 50% of marks in Dissertation Evaluation (Viva-Voce) examination.

7.21 If he fails to fulfill the requirements as specified in 7.21, he will reappear for the Dissertation Viva-Voce examination ***only after three months***. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree, unless he is asked to revise and resubmit his Dissertation Work by the board within a specified time period (within ***four*** years from the date of commencement of his first year first semester).

7.22 The Dissertation Viva-Voce External examination marks must be submitted to the University on the day of the examination.

7.23 ***For mandatory non-credit Audit courses, a student has to secure 40 marks out of 100 marks (i.e. 40% of the marks allotted) in the continuous internal evaluation for passing the subject/course. These marks should also be uploaded along with the internal marks of other subjects.***

7.24 ***No marks or letter grades shall be allotted for mandatory non-credit Audit Courses. Only Pass/Fail shall be indicated in Grade Card.***

8.0 Re-Admission/Re-Registration

8.1 Re-Admission for Discontinued Student

A student, who has discontinued the M. Tech. degree programme due to any reason whatsoever, may be considered for '**readmission'** into the same degree programme (with the same specialization) with the academic regulations of the batch into which he gets readmitted, with prior permission from the authorities concerned, subject to item 6.6.

8.2 If a student is detained in a subject (s) due to shortage of attendance in any semester, he may be permitted to **re-register** for the same subject(s) in the same category (core or elective group) or equivalent subject, if the same subject is not available, as suggested by the Board of Studies of that department, as and when offered in the subsequent semester(s), with the academic regulations of the batch into which he seeks re-registration, with prior permission from the authorities concerned, subject to item 3.2

8.3 ***A candidate shall be given only one-time chance to re-register and attend the classes for a maximum of two subjects in a semester***, if the internal marks secured by a candidate are less than 40% and failed in those subjects but fulfilled the attendance requirement. A candidate must re-register for failed subjects within four weeks of commencement of the class work, in the next academic year and secure the required minimum attendance. In the event of the student taking this chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stand cancelled.

9.0 Examinations and Assessment - The Grading System

9.1 Grades will be awarded to indicate the performance of each student in each Theory Subject, or Lab/Practicals, or Mini Project with Seminar, Dissertation, etc., based on the percentage of marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 7 above, and a corresponding Letter Grade shall be given.

9.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured in a subject/Course (Class Intervals)	**Letter Grade (UGC Guidelines)**	**Grade Points**
90% and above (□ 90%, ≤ 100%)	O (Outstanding)	10
Below 90% but not less than 80% (□80%, <90%)	A^+ (Excellent)	9
Below 80% but not less than 70% (□70%, <80%)	A (Very Good)	8
Below 70% but not less than 60% (□60%, <70%)	B^+ (Good)	7
Below 60% but not less than 50% (□ 50%, <60%)	B (above Average)	6
Below 50% (< 50%)	F (FAIL)	0
Absent	**Ab**	**0**

9.3 A student obtaining **'F'** Grade in any Subject is deemed to have 'failed' and is required to reappear as 'Supplementary Candidate' for the Semester End Examination (SEE), as and when conducted. In such cases, his Internal Marks (CIE Marks) in those subjects will remain as obtained earlier.

9.4 If a student has not appeared for the examinations, '**Ab**' Grade will be allocated to him for any subject and shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' for the

Semester End Examination (SEE), as and when conducted.

9.5 A Letter Grade does not imply any specific marks percentage; it is only the range of percentage of marks.

9.6 In general, a student shall not be permitted to repeat any Subject/ Course (s) only for the sake of 'Grade Improvement' or 'SGPA/ CGPA Improvement'.

9.7 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

9.8 The student passes the Subject/ Course only when he **gets GP ≥ 6 (B Grade or above).**

9.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (□CP) secured from ALL Subjects/ Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

$$\text{SGPA} = \{ \sum_{i=1}^{N} C_i G_i \} / \{ \sum_{i=1}^{N} C_i \} \text{ …. For each Semester,}$$

where 'i' is the Subject indicator index (taking into account all Subjects in a Semester), 'N' is the no. of Subjects 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to the i^{th} Subject, and G_i represents the Grade Points (GP) corresponding to the Letter Grade awarded for that i^{th} Subject.

9.10 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

$$\text{CGPA} = \{ \sum_{j=1}^{M} C_j G_j \} / \{ \sum_{j=1}^{M} C_j \} \text{ … for all S Semesters registered (ie., up to and inclusive of S Semesters, S ≥ 2),}$$

where 'M' is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' for from the 1st Semester onwards upto and inclusive of the Semester S (obviously M > N), 'j' is the Subject indicator index (taking into account all Subjects from 1 to S Semesters), C_j is the no. of Credits allotted to the j^{th} Subject, and G_j represents the Grade Points (GP) corresponding to the Letter Grade awarded for that j^{th} Subject. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

Illustration of calculation of SGPA

Course/Subject	Credits	Letter Grade	Grade points	Credit Points
Course 1	4	A	8	4*8 = 32
Course 2	4	O	10	4*10 = 40
Course 3	4	B	6	4*6 = 24
Course 4	3	B	6	3*6 = 18
Course 5	3	A+	9	3*9 = 27
Course 6	3	B	6	3*6 = 18
	21			159

SGPA = 159/21 = 7.57

Illustration of calculation of CGPA

Semester	Credits	SGPA	Credits * SGPA
Semester I	24	7	24*7 = 168
Semester II	24	6	24*6 = 144
Semester III	24	6.5	24*6.5 = 156
Semester IV	24	6	24*6 = 144
	96		612

CGPA = 612/96 = 6.37

10.0 Award of Degree and Class

10.1 If a student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of **80** Credits (with CGPA □6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with the specialization that he was admitted into.

10.2 Award of Class

After a student has earned the requirements prescribed for the completion of the programme and is eligible for the award of M.Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.75
First Class	6.75≤ CGPA < 7.75
Second Class	6.00≤ CGPA < 6.75

A student with final CGPA (at the end of the **PGP) < 6.00** shall not be eligible for the Award of Degree.

11.0 Withholding of Results

If the student has not paid the dues, if any, to the University or if any case of indiscipline is pending against him, the result and degree of the student will be withheld and he will not be allowed into the next semester.

12.0 General

12.1 **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of

practical work/field work per week.

12.2 **Credit Point:** It is the product of grade point and number of credits for a course.

12.3 Wherever the words "he", "him", "his", occur in the regulations, they shall include "she", "her".

12.4 The academic regulation should be read as a whole for the purpose of any interpretation.

12.5 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the University is final.

12.6 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the University.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR IMPROPER CONDUCT IN EXAMINATIONS

S.No	Nature of Malpractices/Improper conduct	Punishment
	If the candidate:	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject to the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination).	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject to the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent/ any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in- charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any par there of inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in

		connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
   - (i) A show cause notice shall be issued to the college.
   - (ii) Impose a suitable fine on the college.
   - (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

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M.Tech

VLSI&ES

PROGRAMME COURSE STRUCTURE & SYLLABUS

JNTU-GV

COURSE STRUCTURE AND SYLLABUS

M.Tech

in

VLSI & EMBEDDED SYSTEMS (Course Code:68)

And

EMBEDDED SYSTEMS (Course Code:55)

I Year-I Semester

S.NO	Course Code	**Course Title**	**L**	**T**	**P**	**Credits**
1	M255501	CMOS Digital Integrated Circuit Design	3	1	0	4
2	M255502	CMOS Analog Integrated Circuit Design	3	1	0	4
3	M255503	Embedded System Design	3	1	0	4
4	M255504	Scripting Languages	3	1	0	4
	M255505	Soc design				
	M255506	VLSI architectures				
	M255507	Processor Verification				
5	M255508	1. Embedded C	3	1	0	4
	M255509	2. Hardware Software Co-Design				
	M255510	Advanced Computer architecture				
	M255511	IOT				
6	M255512	Analog CMOS Circuit Design Lab	0	1	2	2
7	M255513	Embedded System Design Lab	0	1	2	2
8	M255514	Seminar-I	0	0	2	1
		Total	**15**	**7**	**6**	**25**

I Year II – Semester

S.No	**Course Code**	**Course Title**	**L**	**T**	**P**	**Credits**
1	N255501	CMOS Mixed signal design	3	1	0	4
2	N255502	RTOS	3	1	0	4
3	N255503	Advanced Processors And Controllers	3	1	0	4
4	N255504	Design for Testability	3	1	0	4
	N255505	Physical design and verification				
	N255505	System Verilog & UVM				
	N255507	Low power VLSI Design				
5	N255508	Network security and cryptography	3	1	0	4
	N255509	Embedded Networking				
	N255510	Data Acquisition Systems				
	N255511	Linux Systems with OOPS				
6	N255512	Digital CMOS Circuit Design Lab	0	1	2	2
7	N255513	RTOS Lab	0	1	2	2
8	N255514	Seminar-II	0	0	2	1
		Total	**15**	**7**	**6**	**25**

II YEAR I – SEMESTER

Sl.No.	Course Code	Course Title	L	T	P	C
1	0255501	Research Methodology and IPR / Swayam 12-week MOOC course – RM&IPR	3	0	0	2
2	0255501	Summer Internship/ Industrial Training		-	-	2
3	0255501	Dissertation Part – A	-	-	20	10
		TOTAL	**3**	**-**	**20**	**14**

II YEAR II – SEMESTER

Sl.No.	Course Code	Course Title	L	T	P	C
1	P255501	Dissertation Part – B	0	0	32	16
		Total	**0**	**0**	32	**16**

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

Course overview:

This course provides a thorough understanding of CMOS VLSI design, covering MOS transistors, logic and sequential circuits, arithmetic units, and memory architectures. It emphasizes both static and dynamic behavior, layout strategies, and performance trade-offs in digital integrated circuit design.

Course Objective:

- To understand MOSFET operation under static and dynamic conditions for digital design.
- To analyze CMOS inverter characteristics including power, delay, and energy efficiency.
- To design combinational & sequential logic using various CMOS logic styles.
- To explore arithmetic building blocks focusing on speed and area trade-offs.
- To learn memory architectures including SRAM, ROM, and dynamic memory design techniques.

Course Outcomes:

- Analyze and design MOSFET-based circuits, focusing on static, dynamic, and power characteristics.
- Design combinational logic circuits using static CMOS and dynamic logic with optimization techniques.
- Implement and analyze sequential circuits, including latches, registers, pipelines, and timing considerations.
- Design efficient arithmetic building blocks and memory architectures, focusing on speed and area tradeoffs.

UNIT- I

MOS Transistor Principles & CMOS Inverter: MOSFET characteristics under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter, Static and Dynamic Characteristics, Power, Energy, Energy Delay Parameters, Stick Diagram & Layout Diagrams.

UNIT-II

Combinational Logic Circuits: Static CMOS Design, Different Styles of Logic Circuits, Logical Effort of Complex Gates, Static and Dynamic Properties of Complex Gates, Interconnect Delay, Dynamic Logic Gates.

UNIT-III

Sequential Logic Circuits: Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Non-Bistable Sequential Circuits.

UNIT-IV

Arithmetic Building Blocks: Data Path Circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs.

UNIT-V

Memory Architectures: Memory Architectures and Memory Control Circuits: Read-Only Memories, ROM Cells, Read-Write Memories (RAM), Dynamic Memory Design, 6- Transistor SRAM Cell, Sense Amplifiers.

Text Books:

1. Jan Rabaey, Anantha Chandrakasan, BNikolic, "Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, Feb 2003
2. .N. Weste, K. Eshraghian, "Principles of CMOS VLSI Design",Addision Wesley,2nd Edition, 1993.

Reference Books:

1. MJSmith ,"Application Specific Integrated Circuits",Addisson Wesley,1997
2. **Sung-Mo Kang, Yusuf Leblebici, Chulwoo Kim**, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill Education, **Fourth Edition, 2014 (International) / 2019.**

e-Resources:

1.https://onlinecourses.nptel.ac.in/noc20_ee05/preview

CMOS ANALOG IC DESIGN

Course Overview: This course provides a detailed understanding of MOS devices, CMOS analog sub-circuits, and amplifier design. Topics include MOS transistor modeling, current mirrors, and amplifiers, with a focus on noise analysis and CMOS operational amplifiers. Students will learn about design techniques, compensation methods, and measurement techniques for building efficient and reliable analog circuits.

Course Objective:

- To understand the operation and modeling of MOS transistors in CMOS circuits.
- To design and analyze analog CMOS sub-circuits, such as current mirrors and voltage references.
- To explore single-stage and multi-stage amplifier designs, including gain boosting and cascode techniques.
- To study noise behavior in CMOS amplifiers and mitigate its effects.

Course Outcomes:

- Design basic building blocks of CMOS Analog ICs.
- Carry out the design of single and two stage operational amplifiers and voltage references.
- Determine the device dimensions of each MOSFETs involved.
- Design various amplifiers like differential, current and operational amplifiers.

UNIT- I

MOS Devices and Modeling: The MOS Transistor, Passive Components - Capacitor & Resistor, Integrated Circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT-II

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors - Current Mirror with Beta Helper, Degeneration, Cascode Current Mirror and Wilson Current Mirror, Current and Voltage References, Bandgap Reference.

UNIT- III

Single Stage Amplifier: Common Source Stage with Resistive Load, Diode Connected Load, Triode Load, CS Stage with Source Degeneration, Source Follower, CG Stage, Gain Boosting Techniques, Cascode, Folded Cascode, Choice of Device Models.

UNIT- IV

CMOS Amplifiers and Noise: Inverters, Differential Amplifiers, Cascode Amplifiers. Noise - Statistical Characteristics, Types, Noise in Single-Stage Amplifiers, Noise in Differential Pairs, Noise Bandwidth.

UNIT- V

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of Op Amps.

Text Books:

1. Philip E. Allen and Douglas R. Holberg, "*CMOS Analog Circuit Design"*, Oxford University Press, Third Edition, 2013.
2. Behzad Razavi, "*Design of Analog CMOS Integrated Circuits"*, McGraw-Hill Education, Second Edition, 2016.

Reference Books:

1. David A. Johns and Ken Martin, "*Analog Integrated Circuit Design"*, Wiley Student Edition, 2013.
2. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, "*Analysis and Design of Analog Integrated Circuits"*, Wiley, Sixth Edition, 2024.

e-Reference:

NPTEL: https://www.youtube.com/playlist?list=PLdlPA9pGVVtZ7abJ1MAJc71S2ta OnGux

EMBEDDED SYSTEM DESIGN

Course Overview:

This course provides an in-depth understanding of embedded systems with emphasis on hardware and software co-design. It introduces the ARM architecture, embedded firmware, and programming with Raspberry Pi for real-world interfacing applications. Students will gain knowledge of processor architectures, instruction sets, interfacing techniques, and design methodologies required for building efficient embedded solutions.

Course Objective:

- To introduce the principles and characteristics of embedded systems.
- To understand the architecture of ARM processors and their programming model.
- To provide insights into embedded firmware and its design methodologies.
- To enable students to design embedded applications using Raspberry Pi and Python.
- To develop skills in interfacing sensors and actuators with embedded platforms.

Course Outcomes:

- Understand fundamentals and characteristics of embedded system.
- Analyze ARM architecture, instruction sets, and operating modes.
- Design and develop embedded firmware and interfacing circuits.
- Apply Raspberry Pi for embedded programming and sensor/actuator interfacing.

UNIT- I

Introduction to Embedded Systems

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT-II

Typical Embedded System

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS).Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems. Sensors and Actuators, Communication Interfaces: Onboard and External Interfaces.

UNIT-III

EmbeddedFirmware

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT-IV

ARM Architecture and Instruction Sets

ARM design philosophy, data flow model and core architecture, registers, program status

register, instruction pipeline, interrupts and vector table, operating modes and ARM processor families. Instruction Sets: Data processing instructions, addressing modes, branch,load, store instructions, PSR instructions, conditional instructions.

UNIT-V

Raspberry Pi and Interfacing

Raspberry Pi board and its processor, Programming the Raspberry Pi using Python, Communication facilities on Raspberry Pi (I^2C, SPI, UART), Interfacing of sensors and actuators.

Text Books:

1. Jan Rabaey, Anantha Chandrakasan, BNikolic, "Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, Feb 2003
2. N. Weste, K. Eshraghian, "Principles of CMOS VLSI Design",Addision Wesley,2nd Edition, 1993.

Reference Books:

1. MJSmith ,"Application Specific Integrated Circuits",Addisson Wesley,1997.
2. Sung-Mo Kang, Yusuf Leblebici, "*CMOS Digital Integrated Circuits: Analysis and Design"*, 4th Edition, McGraw-Hill, 2013.

e Resources:

https://onlinecourses.nptel.ac.in/noc25_cs30/preview

SCRIPTING LANGUAGES

Course Overview:

This course introduces scripting languages with applications in VLSI design and CAD automation. It covers PERL, TCL, and PYTHON for data handling, design automation, and tool integration. Students will gain hands-on experience in automating workflows and developing efficient EDA solutions. The course also prepares learners to apply scripting in system development and web applications.

Course Objective:

- To introduce the fundamentals of scripting languages and their role in VLSI design automation.
- To describe PERL concepts for handling large data sets in VLSI/CAD applications.
- To utilize TCL for CAD tool interfacing and automation.
- To interpret the PYTHON language and its role in design, testing, and application development.

Course Outcomes:

- Gain fluency in programming with scripting languages (PERL, TCL, PYTHON).
- Create and execute scripts in PERL/TCL/PYTHON for CAD tool automation and data handling.
- Demonstrate scripting in PERL/TCL/PYTHON for system-level and web applications.
- Analyze security issues, advanced data structures, and tool interfacing using scripting languages.

UNIT- I

Introduction to Scripts and Scripting

Basics of Linux ,Origin of scripting languages , Characteristics, Uses of scripting languages, Applications in VLSI and CAD tools.

Unit-II:

PERL Basics

Introduction to PERL, Names and values, Variables and assignments, Scalar expressions ,Control structures ,Built-in functions, Arrays, Lists, and Hashes ,Simple Input/Output ,Strings ,Regular Expressions , Subroutines , Command-line arguments.

Unit-III:

Advanced PERL

Looping structures ,Advanced Subroutines, Pack and Unpack ,File handling ,Type globs, Eval and References ,Data structures ,Packages, Libraries, and Modules ,Object-Oriented PERL , Tied Variables ,OS Interfacing ,Security Issues.

Unit-IV:

TCL Programming

TCL phenomena ,Philosophy and structure , Syntax and Parser, Variables and data types , Control flow , Data structures , Input/Output ,Procedures , String handling , Patterns , File and Pipe handling , Example applications in EDA.

Unit-V:

PYTHON Programming

Introduction to PYTHON ,Syntax and Statements , Functions ,Built-in Functions and Methods, Modules ,Exception Handling ,Applications of PYTHON in VLSI, system development, and web applications.

Text Books:

1. David Barron, *The World of Scripting Languages*, Wiley Student Edition, 2010.
2. Steve Holden, David Beazley, *PYTHON Web Programming*, New Riders Publications, 2012.

Reference Books:

1. Clif Flynt, *TCL/TK: A Developer's Guide*, Morgan Kaufmann, 2003.
2. Chun, *Core PYTHON Programming*, Pearson Education, 2006.
3. Randal L. Schwartz, *Learning PERL*, O'Reilly Publications, 6th Edition, 2011.
4. Richard Peterson, *Linux: The Complete Reference*, McGraw Hill, 6th Edition, 2008.

e Resources:

https://www.classcentral.com/course/youtube-electronics-linux-programming- scripting-47539

SYSTEM ON CHIP

Course Overview:

This course focuses on System-on-Chip (SoC) design methodologies with hardware-software co-design. It covers processor and memory architecture, bus interconnections, and customization techniques. Students will study design trade-offs involving performance, power, and area in SoC architectures. Real-world case studies like AES encryption and JPEG compression are analyzed for practical insights.

Course Objective:

- To introduce system-level approaches and architectures for SoC design.
- To provide knowledge of processor selection, pipeline optimization, and advanced processor architectures.
- To discuss SoC memory hierarchy, cache design, and processor–memory interactions.
- To study interconnect architectures, SoC standard buses, and reconfiguration techniques, analyze case studies and applications of SoC in cryptography and image processing

Course Outcomes:

- Understand the fundamentals of system architecture, processor architectures, and SoC design approach.
- Analyze processor architectures, pipeline delays, superscalar and VLIW processors.
- Design memory systems including cache hierarchies, scratchpads, and processor- memory interaction models.
- Evaluate interconnect architectures, customization techniques, and reconfiguration trade-offs.

UNIT- I

Introduction to the System Approach

System Architecture – Components of a System, Hardware and Software, Processor Architectures, Memory and Addressing, System-Level Interconnection, SoC Design Approaches, System Complexity.

UNIT-II:

Processor Selection for SoC – Basic Concepts of Processor Architecture & Micro-Architecture, Instruction Handling, Buffers & Pipeline Delay Minimization, Branch Prediction, Vector Processors and Extensions, VLIW Processors, Superscalar Processors.

UNIT-III:

Memory Design in SoC

SoC External and Internal Memory ,Cache Organization & Policies ,Scratchpads ,Write Policies – Line Replacement Strategies ,Split I/D Caches ,Multilevel Caches ,Virtual to Real Translation, SoC Memory Models ,Processor, Memory Interaction Models.

UNIT-IV:

Interconnect Customization and Configuration

Interconnect Architectures – Bus Architectures ,SoC Standard Buses ,Analytic Bus Models, Bus Transaction Analysis ,Customizing Instruction Processors, Reconfiguration Technologies ,Mapping Designs to Reconfigurable Devices ,Instance-Specific Design, Customizable Soft Processors ,Trade-off Analysis of Reconfiguration Overheads.

UNIT-V:

Applications and Case Studies

SoC Design Approach in Applications – AES Algorithm Design and Evaluation – JPEG Compression for Image Processing – Emerging SoC Applications.

Text Books:

1. Michael J. Flynn, Wayne Luk, *Computer System Design: System-on-Chip*, Wiley India Pvt. Ltd.
2. Steve Furber, *ARM System on Chip Architecture*, 2nd Edition, Addison Wesley Professional, 2000.

Reference Books:

1. Ricardo Reis, *Design of System on a Chip: Devices and Components*, Springer, 2004.
2. Jason Andrews, *Co-Verification of Hardware and Software for ARM System on Chip Design*, Newnes, 2004.

e Resources:

1. https://youtu.be/PRQXzjTrCJY?si=Yb60zL9i7AQ7J24S
2. https://youtu.be/FUhCrWoNA2c?si=KLaTDyQy9ME6Kd5t

VLSI ARCHITECTURES

Course Overview:

This course explores programmable logic devices with a focus on FPGA/CPLD architectures and FSM design. It emphasizes architecture-centered design, system-level partitioning, and application-specific implementations. Students will gain knowledge of advanced methodologies like one-hot encoding and ASM-based design. The course also covers controller–datapath design for efficient digital system implementation.

Course Objective:

- To understand programmable logic devices (CPLD/FPGA) and their internal architectures.
- To analyze and compare CPLD/FPGA device families and performance.
- To study finite state machine (FSM) design methodologies and implementation strategies.
- To apply FSM architectures such as one-hot and ASM methods for digital design and develop system-level designs with controller, datapath, and functional partitioning.

Course Outcomes:

- Explain programmable logic device architectures (CPLD, FPGA) and their applications.
- Analyze FPGA/CPLD architectures and evaluate their speed and performance.
- Design finite state machines using PLDs and apply advanced techniques such as one-hot encoding and ASM charts.
- Develop system-level digital designs using controller–datapath partitioning and functional modules.

UNIT–I:

Programmable Logic Devices: Complex Programmable Logic Devices (CPLD): ROM, PLA, PAL, PLD, PGA – Features, programming and applications, Altera MAX 5000/7000 series, Altera FLEX 10000 series CPLD,AMD's CPLD (Mach 1–5), Cypress FLASH 370 device technology, Lattice LSI's 3000 series – Speed, performance, in-system programmability. Introduction to FPGAs: Logic blocks, routing architecture, design flow, technology mapping.

UNIT–II:

FPGA/CPLD Architectures

FPGA/CPLD device architectures: Xilinx XC4000 series, Altera FLEX 8000/10000 series, AT&T ORCA (Optimized Reconfigurable Cell Array),Actel ACT-1, ACT-2, ACT-3 families Comparison of architectures with respect to speed, performance, and area trade-offs.

UNIT–III:

Finite State Machines (FSM) Top-down FSM design, state transition tables, state assignment for FPGAs, Initial state assignment for one-hot encoding, Realization of state machine charts

with PAL, Alternative realization using microprogramming, Linked state machines One-hot state machines, Petri nets for FSM design – concepts, properties, and parallel controllers, Meta-stability and synchronization issues, **Case Study:** FSM-based digital system design.

UNIT–IV:

FSM Architecture

Architectures centered around non-registered PLDs, FSM design using shift registers,One-hot design method and its applications, use of Algorithmic State Machines (ASM) in one- hot design Advantages and trade-offs of FSM-based architecture.

UNIT–V:

System-Level Design

System-level partitioning: Controller, datapath, and functional partitions, design of parallel adder cells and sequential circuits, counters, multiplexers, and system controllers, parallel controllers for high-performance designs, application-oriented system design using FPGAs/CPLDs.

eResources:

1.https://www.youtube.com/playlist?list=PLfMCiCIRnpUnFgNSy0QuOuqIIrG0fe5eD

EMBEDDED C

Course Overview:

This course provides an in-depth understanding of embedded systems, focusing on both hardware and software aspects of design. Students will learn about real-time operating systems (RTOS), hardware-software co-design, interfacing techniques, and design methodologies used in developing reliable and efficient embedded solutions for real-world applications.

Course Objective:

- To provide an overview of Design Principles of Embedded System.
- To provide clear understanding about the role of firmware.
- To understand the necessity of operating systems in correlation with hardware systems.
- To learn the methods of interfacing and synchronization for tasking.

Course Outcomes:

- Apply and analyze the applications in various processors and domains of embedded system.
- Analyze and develop embedded hardware and software development cycles and tools.
- Analyze to understand what a microcomputer, core of the embedded system.
- Analyze to understand different concepts of a RTOS, sensors, memory interface, communication interface.

UNIT- I

Programming Embedded Systems in C:

Introduction, What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions.

Introducing the 8051 Microcontroller Family:

Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements, Clock
frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption, Conclusions.

Unit-II:

Reading Switches: Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions.

Unit-III:

Code Adding Structure to the Code: Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring thegoat-counting example, Further examples, Conclusions.

Unit-IV:

Meeting Real-Time Constraints: Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions.

Unit-V:

Case Study-Intruder Alarm System: Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions.

Text Books:

1. Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008.

Reference Books:

1. PIC MCU C-An introduction to programming, The Microchip PIC in CCS C – Nigel Gardner.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013.
4. An Embedded Software Primer - David E. Simon, Pearson Education.

e Resources:

1. NPTEL : http://nptel.ac.in/courses/108102045/
2. Embedded Systems 1. http://nptel.ac.in/courses/108102045/

HARDWARE SOFTWARE CO DESIGN

Course Overview:

This course introduces the fundamentals of embedded software co-design, focusing on hardware– software partitioning, co-simulation, and verification techniques. Students will learn methodologies, tools, and languages for building efficient and reliable embedded systems through integrated hardware– software development

Course Objective:

- To introduce the fundamentals of embedded hardware-software co-design principles.
- To understand co-design methodologies, partitioning, and synthesis techniques.
- To explore prototyping, emulation, and system-level design languages.
- To study embedded compilation tools and verification methodologies.
- To gain practical experience with embedded co-design case studies and applications.

Course Outcomes:

- Apply co-design methodologies for embedded software-hardware systems.
- Analyze and partition embedded applications into hardware and software components.
- Design and evaluate co-simulation and co-synthesis techniques for embedded systems.
- Develop and verify embedded applications using co-design tools and languages.

UNIT- I

Co- Design Issues :Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co synthesis.

UNIT-II

Prototyping and Emulation

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure **Target Architectures:**Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III:

Compilation Techniques and Tools for Embedded Processor Architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT-IV:

Design Specification and Verification

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, Interface verification.

UNIT-V:

Languages for System-Level Specification and Design-I

System-level specification, design representation for system level synthesis, system level specification languages.

Languages for System-Level Specification and Design-II

Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system..

Text Books:

1.Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.

2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.

Reference Books:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer Publications.

e-Resources:

1.NPTEL : https://nptel.ac.in/courses/106103182

ADVANCED COMPUTER ARCHITECTURE

Course Overview:

This course introduces the fundamentals of parallel computer architecture and models. It covers processor technologies, memory hierarchies, pipelining, and superscalar techniques. Students learn about parallelism, scheduling, interconnection networks, and performance metrics.

Course Objective:

- To Understand the Foundations of Parallel Computing.
- To Analyze Parallel Program Design and System Interconnects.
- To Explore Processor and Memory Architectures.
- To Examine Advanced Parallel Processing Techniques.

Course Outcomes:

- **Understand and compare** various parallel computer models, including multiprocessors and multicomputers.
- **Analyze and apply** program partitioning, scheduling techniques, and interconnect architectures for achieving effective parallelism in computing systems.
- **Evaluate** advanced processor technologies, memory hierarchy, cache and shared memory organizations to optimize processor and memory interactions in high-performance systems.
- **Design and assess** pipelining techniques, superscalar architectures, and multithreading models for efficient execution in multiprocessor and vector processing systems.

UNIT- I

Parallel Computer Models – System attributes to performance, Multiprocessors and Multicomputers,

Classifications of Architectures, Multi vector and SIMD Computers, Architecture development tracks.

UNIT-II:

Program and Network Properties- Conditions for parallelism, Program partitioning and Scheduling, Program flow mechanisms, System interconnect architectures, Performance metrics and measures, Parallel Processing Applications.

UNIT-III:

Processors and Memory Hierarchy- Advanced Processor Technology, Superscalar and Vector processors, Memory hierarchy technology, Virtual Memory, Backplane bus systems, Cache memory organizations, Shared memory organizations.

UNIT-IV:

Pipelining and Superscalar Techniques Linear Pipeline processors, Nonlinear pipeline processors, Instruction pipeline design, Arithmetic pipeline design, Superscalar and Super Pipeline Design.

UNIT-V:

Multiprocessors and Multicomputers Multiprocessor System Interconnects, Cache Coherence and Synchronization mechanisms, Three generations of Multicomputers, Message passing mechanisms, Vector Processing principles, Principles of Multithreading.

Text Books:

1. Hwang kai, "Advanced Computer Architecture", McGraw-Hill, 2001.
Patterson, David and Hennessy John, Morgn Kaufmann, "Computer Architecture",2001.

Reference Books:

1. William Stallings, Computer Organization and Architecture, 8th Edition, Prentice-Hall India, 2010.
2. David A Patterson and John L. Hennesey, Computer Organization and Design, 4th Edition, Elsevier India, 2011.
3. Andrew S Tanenbaum and James R Goodman, Structured Computer Organization, 5th Edition Prentice Hall India, 2009.

e-Resources:

1. NPTEL : https://onlinecourses.nptel.ac.in/noc25_cs01/preview

INTERNET OF THINGS

Course Overview:

This course introduces Embedded Systems and IoT architectures, covering ARM microcontroller programming, Arduino, Raspberry Pi, and Python-based sensor/actuator interfacing. It also explores IoT platforms, cloud integration, and real-world application deployment using tools like IBM Watson and Node-RED.

Course Objective:

- To identify problems that are amenable to solution by AI methods, and which AI methods may be suited to solving a given problem.
- To formalize a given problem in the language/framework of different AI methods (e.g., as a search problem, as a constraint satisfaction problem, as a planning problem, as a Markov decision process, etc).
- To implement basic AI algorithms (e.g., standard search algorithms or dynamic programming).
- To design and carry out an empirical evaluation of different algorithms on problem formalization, and state the conclusions that the evaluation supports.

Course Outcomes:

- Demonstrate knowledge and understanding of the security and ethical issues of the Internet of Things.
- Conceptually identify vulnerabilities, including recent attacks, involving the Internet of Thing.
- Develop critical thinking skills.
- Compare and contrast the threat environment based on industry and/or device type.

UNIT– I

Introduction to Embedded Systems and Internet of Things (IOT) :

Architecture of Embedded Systems, Embedded Systems Development process, Architecture of Internet of Things, applications of Embedded Systems and IoT, Design Methodology for IOT Products.

UNIT–II

ARM Microcontrollers Architecture and Programming Architecture, Instruction set, Programming ports, Timer/Counter, Serial communication, Interrupts in C, Introduction ARM mBed platform.

UNIT- III

Overview of Open Source Hardware and Its relevance to IOT Introduction and Programming Arduino Development Board, Working with Sensor Integration, Interfacing Input/Output devices (LCD,Key Pad, LED Matrix etc)

UNIT IV

Fundamentals of Python Programming & Raspeberry PI Introduction to python programming, Working with functions, classes, REST full Web Services, Client Libraries, Introduction & programming Raspberry Pi3,Integrating Input Output devices with Raspberry Pi3.

UNIT V

IOT: Technologies, Standards and Tools

Fundamental characteristics and high level requirements of IoT, IoT Reference models, Introduction to Communication Technologies & Protocols of IoT: BLE, Wi-Fi, LoRA, 3G/4G Technologies and HTTP, MQTT, CoAP protocols, Relevant Practical's on above technologies

IOT Platform: Cloud Computing Platforms for IOT Development (IBM CLOUD – Register in IBM Blue mix website) IOT Platform Architecture (IBM Internet of Things & Watson Platforms), API Endpoints for Platform Services, Devices Creation and Data Transmission, Introduction to NODE-RED and Application deployment.

Text Books :

1. Internet of Things: A Hands-On Approach by by Arsheep Bahga, Vijay Madisetti
2. Embedded Real Time Systems: Concepts, Design and Programming‖ by Dr.K.V.K.K.Prasad, Dream Tech Publication, 2003.

Reference Books:

1.Embedded Systems: Real-Time Interfacing to Arm(r) Cortex -M Microcontrollers: volume-1 & 2 by Jonathan W Valvano.
2. Designing the Internet of Things‖ by Adrian McEwen, Hakim Cassimally, Wiley Publications, 2012

e Resources:

1. http://www.slideshare.net/RealTimeInnovations/io-34485340
2. http://internetofthings.electronicsforu.com

ANALOG CMOS CIRCUIT DESIGN LAB

Course Overview: This lab course focuses on designing and simulating analog CMOS circuits using industry-standard EDA tools. Students gain hands-on experience in schematic design, layout, simulation, and verification, enhancing their understanding of VLSI design methodologies and analog integrated circuit performance optimization.

Course Objective:

- To understand CMOS analog design using EDA tools and techniques.
- To develop schematics and layouts for optimized analog circuit performance.
- To perform simulations verifying functionality of pre-layout and post-layout designs.
- To apply physical verification ensuring correctness and manufacturability of layouts.

Course Outcomes:

- Apply VLSI design methodologies using Mentor Graphics tools to design and verify IC circuits.
- Analyze CMOS analog circuits' role in full-custom IC design flows for performance optimization.
- Apply physical verification techniques in layout design to ensure design correctness and manufacturability.
- Create pre-layout and post-layout simulations to validate and optimize VLSI designs for functionality.

List of Experiments:

Exp No.	Experiment Name
1	MOS Device Characterization and parametric analysis
2	Common Source Amplifier.
3	Common Source Amplifier with source degeneration.
4	Cascode amplifier.
5	Simple current mirror.
6	Cascode current mirror.
7	Wilson current mirror.
8	Differential Amplifier.
9	Operational Amplifier.
10	Sample and Hold Circuit.
11	Direct-conversion ADC.
12	R-2R Ladder Type DAC.

Lab Requirements:

Software:

Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator/
Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

EMBEDDED SYSTEM DESIGN LAB

Course Objectives :

IDE for Embedded System Design using MSP430; Interfacing Switch & LED; Timers-WDT, Configuring, Programming; ADC-usage; Power down modes; DAC; PWM Generator; Networking - SPI, Wi-Fi.

Course Outcomes :

- Demonstrate knowledge in designing complex energy efficient embedded systems.
- Analyze usage of various on-chip resources like GPIO, Timers, Interrupts, ADC, DAC, Comparator, SPI.
- Apply appropriate techniques, resources, and CCSV6 based IDE for modeling embedded systems with understanding of limitations.
- Work individually and in a group to develop embedded systems.

List of Experiments:

Exp No.	Experiment Name
1	Introduction to MSP430 launch pad and Programming Environment.
2	Read input from switch and Automatic control/flash LED (soft-ware delay).
3	Interrupts programming example using GPIO.
4	Configure watchdog timer in watchdog & interval mode.
5	Configure timer block for signal generation (with given frequency).
6	Read Temperature of MSP430 with the help of ADC.
7	Test various Power Down modes in MSP430.
8	PWM Generator.
9	Use Comparator to compare the signal threshold level.
10	Speed Control of DC Motor.
11	Master slave communication between MSPs using SPI.
12	Networking MSPs using Wi-Fi.

TOOL REQUIREMENT:

Code Composer Studio Version 6, MSP430 based launch pads, Wi-Fi booster pack.

CMOS MIXED SIGNAL DESIGN

Course Overview: This course covers advanced topics in analog CMOS design, including two-stage op-amp design, switched capacitor circuits, sample-and-hold circuits, comparators, data converters, and phase-locked loops (PLLs). Emphasis is placed on circuit analysis, noise reduction, parasitic effects, and performance limitations. Students will learn practical design strategies for high-performance analog circuits.

Course Objective:

- To design and analyze two-stage operational amplifiers, focusing on parasitic effects and biasing.
- To explore switched capacitor circuits and their applications in filter design and integrators.
- To understand the principles and design of comparators, including issues like propagation delay and slew rate.
- To study data converters and PLLs, emphasizing performance limitations, noise, and circuit optimization.

Course Outcomes:

- Understand the necessity of mixed signal syatem.
- Analyze Op-Amp to meet the mixed signal specifications.
- Design CMOS comparators to meet the high- speed requirements of digital circuitry.
- Develop efficient data converter circuits for mixed signal systems.

UNIT- I

Two-Stage OP-AMP Design: Parasitic Effects on Design of Two-Stage OP-AMP, Wide-Swing Cascode Current Mirrors, Design of Rugged Biasing Circuit with Temperature-Independent Compensation, Challenges in Mixed-Signal Circuit Design.

Switched Capacitor Circuits : Constituents: Op-Amp, Capacitors, Switches, Non- overlapping Clocks; Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic-Insensitive Integrators, Signal-Flow- Graph Analysis, Design of Filters Based on Switched Capacitor Circuits.

UNIT- II

Sample-and-Hold Circuit: Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Charge-Injection Errors, Making Charge-Injection Signal Independent, Minimizing Errors Due to Charge-Injection, Effect of Offset and Application of Switched Capacitor Circuits to Minimize Offset Errors, Parasitic Effects.

UNIT- III

Comparators: Ideal Comparator, Practical Model of Comparator, Resolving Capability, Propagation Delay, Small Signal Analysis, Conditions for Slewing, Evaluation of Propagation Delay for Single Pole and Two Pole Comparators, Design of Linear Response Comparators,

Slew-Rate Limited Comparators, Comparators with Positive Feedback, Analysis of Latched Comparators, Architecture of High-Speed Comparators, Self-Biased
Comparators, Push Pull Comparators.

UNIT- IV

Data Converters: Classification, Ideal D/A Converter, Ideal A/D Converter, Quantization Noise: Deterministic and Stochastic Approach, Signed Codes, Performance Limitations: Resolution, Offset and Gain Error, Accuracy and Linearity, Integrating Converters, Design of Successive-Approximation Converters, DAC-Based and Charge-Redistribution SAR, Interleaved, Pipelined, Flash, Principles of Sigma-Delta ADC, Testing of Data Converters.

UNIT- V

PLL and Oscillators: Basic PLL Architecture, VCO, Divider, Phase Detector, Loop Filter, PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model, Limitations, PLL Characterization and Design Example, Jitter and Phase Noise: Period Jitter, Cycle Jitter, Adjacent Period Jitter, Spectral Representations and PDF of Jitter, Ring and LC Oscillators, Phase Noise in Oscillators and PLLs.

Text Book:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuits"McGraw Hill Education, 2017, 2nd Edition.

Referenc Books:

1. Roubik Gregorian and Gabor C. Temes, Analog MOS integrated circuits for signal processing, Wiley, 1986.
2. Roubik Gregorian, Introduction to CMOS Op-Amps and Comparators, Wiley, 2008.

e-Reference:

NPTELCourses(https://onlinecourses.nptel.ac.in/noc22_ee34/preview)

RTOS

Course Overview:

This course explores Real-Time Operating Systems (RTOS) with a focus on embedded systems. Key topics include task scheduling, interrupt handling, and memory management. Students gain hands-on experience with RTOS like µC/OS-II, VxWorks, and RT Linux. Practical skills in Unix/Linux programming and real-time application development are emphasized.

Course Objective:

- To introduce the fundamental services and features of operating systems, with emphasis on real-time constraints.
- To familiarize students with programming concepts of different RTOS used in embedded systems.
- To provide knowledge of program modeling through real-world case studies in embedded systems.
- To develop skills for RTOS-based application development and target image creation using Linux and to understand and implement real-time programming concepts using RT Linux and its APIs.

Course Outcomes:

- Explain the architecture, services, and functions of operating systems in a real-time environment.
- Demonstrate the ability to write and analyze programs using µC/OS-II, VxWorks, Windows CE, and RT Linux.
- Model and evaluate embedded system applications through case studies like smart cards, mobile phones, etc.
- Develop and debug RTOS-based applications and perform target image creation using Linux tools.

UNIT- I

Introduction: OS Services, Process Management, Timer Functions, Event Functions, Memory Management, Device, File and IO Systems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls, Real-Time Operating Systems, Basic Design Using an RTOS, RTOS Task Scheduling Models, Interrupt Latency and Response of the Tasks as Performance Metrics, OS Security Issues.

UNIT-II:

RTOS Programming: Basic Functions and Types of RTOS for Embedded Systems, RTOS mCOS- II, RTOS Vx Works, Programming concepts of above RTOS with relevant Examples, Programming concepts of RTOS Windows CE, RTOS Linux 2.6.x and RTOS RT Linux.

UNIT-III:

Program Modeling – Case Studies: Case study of digital camera hardware and software

architecture, Case Study of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of Embedded System for a Smart Card, Case Study of Embedded System of Mobile Phone Software for Key Inputs..

UNIT-IV:

Target Image Creation & Programming in Linux: Operating System Software, Target Image Creation for Window XP Embedded, Porting RTOS on a Micro Controller based Development Board. Overview and programming concepts of Unix/Linux Programming, Shell Programming, System Programming.

UNIT-V:

Programming in RT Linux: Overview of RT Linux, Core RT Linux API, Program to display a message periodically, semaphore management, Mutex, Management, Case Study of Appliance Control by RT Linux System.

Text Books:

1 Rajkamal: "Embedded Systems-Architecture, Programming and Design", Tata McGraw Hill Publications, Second Edition, 2008.

2. Dr. K.V.K.K. Prasad: "Embedded/Real-Time Systems" Dream Tech Publications, 2005 Edition, Black pad book.

Reference Books:

1. Labrosse, "Embedding system building blocks ", CMP publishers.
2. Rob Williams," Real time Systems Development", Butterworth Heinemann Publications.

e-Resources:

1. https://nptel.ac.in/courses/106105172

ADVANCED PROCESSORS AND CONTROLLERS

Course Overview:

This course introduces the architecture and programming of modern processors including the Pentium, ARM, Motorola 68HC11, and PIC microcontrollers. It covers instruction sets, operating modes, interrupts, and memory management. Emphasis is placed on application development using ARM processors and embedded systems concepts..

Course Objective:

- To understand the architecture, instruction set, and operation of general-purpose and embedded processors.
- To explore the ARM architecture and its application in high-performance embedded systems.
- To develop practical skills in programming microcontrollers (ARM, 68HC11, PIC) in Assembly and C.
- To understand peripheral interfacing, interrupt handling, and memory management in embedded systems.

Course Outcomes:

- Describe CPU architectures, instruction sets, and basic operations of Pentium and RISC processors.
- Analyze ARM architecture, instruction cycle timing, and implement optimized embedded programs.
- Develop ARM-based applications including DSP functions, bootloaders, and peripheral interface routines.
- Program and interface with microcontrollers (68HC11, PIC) using C and assembly language.

UNIT- I

High Performance Cisc Architecture –Pentium CPU Architecture - Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging –Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

UNIT-II:

High Performance Risc Architecture

ARM Arcon RISC Machine – Architectural Inheritance – Core & Architectures - Registers – Pipeline- Interrupts – ARM organization - ARM processor family – Co-processors - ARM instruction set- Thumb Instruction set - Instruction cycle timings - The ARM Programmer‟s model – ARM Development tools – ARM Assembly Language Programming – C programming – Optimizing ARM Assembly Code – Optimized Primitives.

UNIT-III:

Arm Application Development

Introduction to DSP on ARM –FIR filter – IIR filter – Discrete fourier transform – Exception handling-Interrupts –Interrupt handling schemes- Firmware and boot loader – Embedded Operating systems-Integrated Development Environment- STDIO Libraries – Peripheral Interface – Application of ARM Processor - Caches – Memory protection Units – Memory Management units – Future ARM Technologies.

UNIT-IV:

Motorola 68hc11 Microcontrollers

Instruction set addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART.

UNIT-V:

Pic Microcontroller

CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter – PWM and introduction to C-Compilers.

Text Books:

1.Andrew N.Sloss, Dominic Symes and Chris Wright " ARM System Developer"s Guide : Designing and Optimizing System Software" , First edition, Morgan Kaufmann Publishers, 2004.

2.Steve Furber , "ARM System –On –Chip architecture", Addision Wesley, 2000.

Reference Books:

1. Daniel Tabak , "Advanced Microprocessors", Mc Graw Hill. Inc., 1995

2. James L. Antonakos , " The Pentium Microprocessor", Pearson Education, 1997.

e-Resources:

1. https://onlinecourses.nptel.ac.in/noc22_ee12/preview

DESIGN FOR TESTABILITY

Course Overview:

This course covers the principles and techniques for designing testable digital systems in VLSI. It includes fault modeling, logic and fault simulation, and testability analysis. Students learn scan-based design, BIST, and boundary scan techniques. Emphasis is placed on creating reliable, manufacturable systems through effective test design..

Course Objective:

- To understand the fundamental concepts and philosophies of digital system testing.
- To explore various fault modeling and simulation techniques for test evaluation.
- To introduce and apply scan-based design and testability enhancement techniques.
- To analyze and implement BIST and boundary scan architectures in digital systems.

Course Outcomes:

- Explain various fault models, simulation techniques, and their role in VLSI testing.
- Apply testability analysis methods and scan-based design techniques to digital circuits.
- Analyze and implement built-in self-test (BIST) architectures for logic and memory circuits.
- Design and configure boundary scan systems using IEEE standards and interpret BSDL specifications.

UNIT- I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II:

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT-III:

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV:

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V:

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary

Scan Description Language: BDSL Description Components, Pin Descriptions.

Text Books:

1. M.L. Bushnell, V. D. Agrawal, “Essential of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Publishers.

Reference Books:

1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design”, Jaico Publishing House.
2. P. K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

e Resources:

https://nptel.ac.in/courses/117105137

PHYSICAL DESIGN VERIFICATION

Course Overview: This course covers VLSI physical design, focusing on design cycles, fabrication processes, and layout techniques. Topics include design styles, interconnect delay, complexity issues, graph algorithms, and data structures for layout editors. It also explores partitioning, floor planning, pin assignment, and routing algorithms, equipping students with tools for efficient VLSI design.

Course Objective:

- To understand the VLSI design and physical design cycles, including fabrication and layout processes.
- To explore design styles and interconnect issues, focusing on noise, crosstalk, and yield.
- To study graph algorithms and data structures for solving physical design problems.
- To learn partitioning, floor planning, and routing algorithms for efficient VLSI design.

Course Outcomes:

- Understand the relationship between design automation algorithms and Various constraints posed by VLSI fabrication and design technology.
- Adapt the design algorithms to meet the critical design parameters.
- Identify layout optimization techniques and map them to the algorithms.
- Develop proto-type EDA tool and test its efficacy.

UNIT- I

VLSI Design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication. Design styles: Full Custom, Standard Cell, Gate Arrays, Field Programmable Gate Arrays, Sea of Gates and Comparison, System Packaging Styles, Multi- Chip Modules. Design Rules, Layout of Basic Devices, Fabrication Process and Its Impact on Physical Design, Interconnect Delay, Noise and Crosstalk, Yield and Fabrication Cost.

UNIT- II

Factors, Complexity Issues and NP-hard Problems. Basic Algorithms (Graph and Computational Geometry): Graph Search Algorithms, Spanning Tree Algorithms, Shortest Path Algorithms, Matching Algorithms, Min-Cut and Max-Cut Algorithms, Steiner Tree Algorithms.

UNIT- III

Basic Data Structures: Atomic Operations for Layout Editors, Linked List of Blocks, Bin Based Methods, Neighbour Pointers, Corner Stitching, Multi-Layer Operations.

UNIT- IV

Graph Algorithms for Physical Design: Classes of Graphs, Graphs Related to a Set of Lines, Graphs Related to a Set of Rectangles, Graph Problems in Physical Design, Maximum Clique and Minimum Coloring, Maximum k-Independent Set Algorithm, Algorithms for Circle Graphs.

UNIT- V

Partitioning Algorithms: Design Style Specific Partitioning Problems, Group Migrated Algorithms, Simulated Annealing and Evolution. Floor Planning and Pin Assignment, Routing and Placement Algorithms.

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008.

Reference Books:

1. "CMOS VLSI Design: A Circuits and Systems Perspective" by Neil H. E. Weste and David Harris.
2. "VLSI Physical Design: From Graph Partitioning to Timing Closure" by K. D. Meade and L. F. D. DeMicheli.

e-Reference:

NPTEL Courses **(https://nptel.ac.in/courses/106103016)**

SYSTEM VERILOG & UVM

Course Overview:

This course introduces System Verilog and UVM for advanced hardware verification. It covers testbench design, constrained random verification, and functional coverage techniques. Students learn to create assertions and apply formal verification methods to debug designs. The course also addresses hardware security threats and countermeasures using modern verification tools.

Course Objective:

- To introduce students to digital design verification using System Verilog and object- oriented programming.
- To develop skills in building layered, coverage-driven testbenches using System Verilog and UVM.
- To understand formal verification concepts, assertions, and concurrency mechanisms for robust bug detection.
- To explore the dimensions of hardware security including threats like IP piracy and Trojans, and mitigation strategies.

Course Outcomes:

- Understand the principles of System Verilog verification, including testbench design and OOP features.
- Apply constrained random verification and functional coverage to evaluate DUT behavior using System Verilog & UVM.
- Analyze and construct assertions and formal verification strategies to detect and debug design flaws.
- Identify and assess hardware security threats and apply suitable countermeasures using modern verification tools.

UNIT- I

System Verilog Design Verification-I: The concept of Device under test (DUT), Complexity of verification, lexical elements of system Verilog (SV), Layered testbench and SV verification environment.

Unit-II:

System Verilog Design Verification-II: - Basics of SV testbench, concurrency in system Verilog, object oriented programming, encapsulation and randomization.

Unit-III:

System Verilog Design Verification –III: - Inter-thread communications, mailbox, code coverage, functional coverage and building efficient SV testbenches. System Verilog UVM.

Unit-IV:

Formal Verification (FV): -Importance of FV, Challenges in implementing FV, Boolean Algebra, Boolean satisfiability, Basic assertion concepts, immediate assertions, concurrent assertions, Sequences, clocks, resets and coverage.

Unit-V:

Hardware Security: - Reasons for raise of hardware security issues, IC Counterfeiting, IP piracy, Hardware Trojans, Debug security and applications of Physical Unclonable Functions(PUF).

Text Books:

1. System Verilog for Verification: A Guide to Learning the Testbench Language Features by Chris Spear , Greg Tumbush, Springer; 3rd ed. 2012 edition.
2. System Verilog Assertions and Functional Coverage: Guide to Language, Methodology and Applications, by Ashok B. Mehta, Springer; 2014 edition.

Reference Books:

1.Formal Verification: An Essential Toolkit for Modern VLSI Design 1st Edition by Erik Seligman, Tom Schubert , M V Achutha Kiran Kumar, Morgan Kaufmann; 2015.
2. Clifford E. Cummings, "System verilog Assertions - Bind files & Best Known Practices for Simple SVA Usage"

e-Resources:

1. https://onlinecourses.nptel.ac.in/noc21

LOW POWER VLSI DESIGN

Course Overview:
This course focuses on power-aware design methodologies essential for modern VLSI systems. It examines dynamic and static power dissipation in digital circuits and strategies to minimize them. Topics include voltage scaling, leakage reduction, and efficient clocking. Students will also learn power estimation and optimization through analysis and simulation.

Course Objectives:
- To understand the different sources and types of power dissipation in digital CMOS circuits.
- To Analyze power dissipation characteristics at gate-level and circuit-level.
- To Explore voltage scaling and its challenges as a means for reducing power.
- To Apply architectural techniques such as parallelism and pipelining for low-power design.

Course Outcomes:
- Identify the causes of dynamic and static power dissipation and quantify them using analytical models.
- Apply supply voltage scaling and architectural techniques like pipelining and parallelism to reduce power consumption.
- Analyze and implement switching activity reduction techniques such as clock gating, bus encoding, and FSM optimization.
- Use simulation-based tools and modeling approaches (e.g., SPICE, Monte Carlo) to estimate and minimize power in VLSI circuits.

UNIT- I

Sources of Power Dissipation: Introduction, Short-Circuit Power Dissipation, Switching Power Dissipation, Dynamic Power for Complex Gate, Reduced Voltage Swing, Switching Activity, Leakage Power Dissipation, p–n Junction Reverse-Biased Current, Band-Band Tunneling Current, Subthreshold Leakage Current, Short-Channel Effects.

UNIT-II:

Supply Voltage Scaling for Low Power: Device Feature Size Scaling, Constant-Field Scaling, Constant-Voltage Scaling, Architectural- Level Approaches: Parallelism for Low Power, Pipelining for Low Power, Combining Parallelism with Pipelining, Voltage Scaling Using High-Level Transformations: Multilevel Voltage Scaling Challenges in MVS Voltage Scaling Interfaces, Static Timing Analysis
Dynamic Voltage and Frequency Scaling.

UNIT-III:

Switched Capacitance Minimization: Probabilistic Power Analysis: Random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, Bus Encoding: Gray Coding, One-Hot Coding, Bus- Inversion, T0 Coding, Clock Gating, Gated-Clock FSMs FSM State Encoding, FSM Partitioning, Precomputation, Glitching Power Minimization.

Unit-IV:

Leakage Power Minimization: Fabrication of Multiple Threshold Voltages, Multiple Channel Doping, Multiple Oxide CMOS, Multiple Channel Length, Multiple Body Bias, VTCMOS Approach, MTCMOS Approach, Power Gating, Clock Gating Versus Power Gating, Power-Gating Issues, Isolation Strategy, State Retention Strategy, Power-Gating Controller, Power Management, Combining DVFS and Power Management

Unit-V:

Low power clock distribution & Simulation Power Analysis: Low power clock distribution: Power dissipation in clock distribution, single driver versus distributed buffers, Zero skew versus tolerable skew, chip and package co design for clock network. Simulation Power Analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, architecture level analysis, data correlation analysis of DSP systems, Monte Carlo Simulation.

Text Books:

1. Low-Power VLSI Circuits and Systems, Ajit Pal, SPRINGER PUBLISHERS
2. Practical Low Power Digital VLSI Design ,Gary Yeap Motorola, Springer Science Business Media, Llc.

Reference Books:

1. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998. 2
2. Massoud Pedram, Jan M. Rabaey,"Low power design methodologies ", Kluwer Academic Publishers.
3. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.

e Resources:

https://nptel.ac.in/courses/106105034

NETWORK SECURITY AND CRYPTOGRAPHY

Course Overview: This course covers the principles and techniques used to secure information systems and networks. It includes classical and modern cryptography, authentication, and secure communication protocols. Students learn about threats like intrusions and malware, and countermeasures like firewalls and trusted systems. Emphasis is placed on both theoretical foundations and practical applications of cybersecurity.

Course Objective:

- To understand the fundamental concepts of cryptography and network security mechanisms.
- To explore classical and modern encryption algorithms and their security properties.
- To learn public key cryptographic systems, key exchange protocols, and associated number theory.
- To understand message authentication, digital signatures, and secure communication protocols.
- To study real-world network security applications such as IP security, web security, email security, and threat mitigation.

Course Outcomes:

- Explain the fundamental principles of cryptography and classical encryption techniques.
- Apply symmetric and asymmetric encryption algorithms in securing data communication.
- Analyze and evaluate cryptographic techniques such as RSA, Diffie-Hellman, and digital signatures for secure systems.
- Design and implement secure communication mechanisms using protocols like SSL, IPsec, and authentication systems.

UNIT- I

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques. Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

UNIT-II:

Encryption Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers. Conventional Encryption :Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation. 12 3 Public Key Cryptography: Principles, RSA Algorithm, Key Management.

UNIT-III:

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography. Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

UNIT-IV:

Message Authentication and Hash Functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs. Hash and Mac Algorithms. MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. Digital signatures and Authentication protocols: Digital signatures, Authentication Protocols, Digital signature standards. Authentication Applications: Kerberos, X.509 directory Authentication service. Electronic Mail Security: Pretty Good Privacy, S/MIME..

UNIT-V:

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management. Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction. Intruders, Viruses and Worms Intruders, Viruses and Related threats. Fire Walls: Fire wall Design Principles, Trusted systems.

Text Books:

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education.
2. Network Security Essentials (Applications and Standards) by William Stallings Pearson Education.

Reference Books:

1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
2. Network Security - Private Communication in a Public World by Charlie Kaufman, Radia Perlman and Mike Speciner, Pearson/PHI.
3. Principles of Information Security, Whitman, Thomson.
4. Network Security: The complete reference, Robert Bragg, Mark Rhodes, TMH
5. Introduction to Cryptography, Buchmann, Springer.

e Resources:

https://nptel.ac.in/courses/106105031

EMBEDDED NETWORKING

Course Overview:

This course covers the fundamentals and advanced concepts of embedded networking in both wired and wireless systems. Topics include serial, parallel, USB, CAN, and Ethernet communication protocols. Students explore wireless sensor networks and secure communication in embedded systems. Practical learning involves programming microcontrollers like the PIC18 for network interfacing and design.

Course Objective:

- To understand the principles and applications of serial, parallel, and bus-based communication in embedded systems.
- To explore USB and CAN bus communication protocols and implement simple applications using micro controllers.
- To analyze and implement Ethernet-based communication for embedded systems.
- To design and secure embedded systems capable of TCP/IP networking and internet-based communication.

Course Outcomes:

- Explain various embedded communication protocols including RS232, SPI, I2C, and PCI.
- Develop and implement USB and CAN- based communication using PIC microcontrollers.
- Design Ethernet-enabled embedded systems using TCP/IP and serve dynamic web content.
- Analyze and compare wireless embedded networking protocols with focus on MAC and routing efficiency..

UNIT- I

Embedded Communication Protocols:

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT-II:

USB and CAN Bus: USB bus-Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing – Types of errors – Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT-III:

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers – Using the internet in local and internet communications – Inside the

Internet Protocol.

UNIT-IV:

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT-V:

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols – SMAC – Energy efficient and robust routing – Data Centric routing.

Text Books:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

Reference Books:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.

e Resources:

https://onlinecourses.nptel.ac.in/noc22_cs93/preview

DATA ACQUISITION SYSTEMS

Course Overview:

This course offers an in-depth study of data acquisition systems (DAS), focusing on ADCs and DACs. It explores converter classifications, design principles, and advanced configurations like high-speed and hybrid systems. Practical applications in communication, DSP, and instrumentation are covered. Key topics include error budgeting, noise reduction, and microprocessor interfacing.

Course Objective:

- To understand the principles and classification of various ADC architectures and their operating mechanisms.
- To analyze non-linear data converter configurations and evaluate
- their applications in real-time systems.
- To design different types of DACs and apply them in programmable and signal- processing systems.
- To valuate performance parameters, error sources, and noise reduction techniques in data acquisition systems.

Course Outcomes:

- Classify different ADC types and explain their working principles.
- Analyze and develop embedded hardware and software development cycles and tools
- Analyze to understand what a microcomputer, core of the embedded system
- Analyze to understand different concepts of a RTOS, sensors, memory interface, communication interface.

UNIT- I

INTRODUCTION: Objective of a DAS, single channel DAS, Multi-channel DAS, Components used in DAS- Converter Characteristics-Resolution-Non-linearity, settling time, Monotonícity.

Unit-II:

ANALOG TO DIGITAL CONVERTERS (ADCS):**Classification of A/D converters**:Parallel feedback, successive approximation, Ramp comparison, Dual slope Integration,voltage to frequency, Voltage to Time, logarithmic types of ADCS.

Non-Linear Data Converters NDC: Basic NDC configurations - Some common NDACS and NADCS, Programmable non-linear ADCS, NADC using optimal sized ROM High speed hybrid NADC, PLS based NADC, Switched capacitor NDCS.

ADC Voice Applications: Data Acquisition systems - Digital signal processing systems - PCM systems, Test and measurement instruments, electronic weighing machines.

Unit-III:

DIGITAL TO ANALOG CONVERTERS (DACS): Principles and design of- Parallel R 2R, Weighted resistor, inverted ladder, D/A decoding-Codes other than ordinary binary. Data

Converter Applications: DAC applications - Digitally programmable V/I sources - Arbitrary waveform generators- Digitally programmable gain amplifiers, Analog multipliers/ dividers, Analog delay lines.

Unit-IV:

Monolithic data converters: Typical study of monolithic DACS and ADCS. Interfacing of DACS and ADCS to a uP.

Unit-V:

Error budget of DACS and ADCS: Error sources, error reduction and noise reduction techniques in DAS. Error budget analysis of DAS, case study of a DAC and an ADC.

Text Books:

1. Electronic data converters fundamentals and applications, Dinesh K. Anvekar, B.S. Sonde - Tata McGraw Hill.
2. Electronic Analog/ Digital conversions - Hermann Schmid- Tata McGraw Hill.

Reference Books:

1.E.R. Hanateck, User's Handbook of D/A and A/D converters – Wiley.
2. Electronic instrumentation by HS Kalsi- TMH 2 nd Edition, 2004.
3. Data converters by G.B. Clayton.

e-Resources:

https://www.youtube.com/watch?v=WwQSfk6SSSo&t=15s

LINUX PROGRAMMING AND OOPS

Course Overview:

This course provides students to Linux operating system fundamentals including file systems, commands, utilities, shell programming, and memory management. It also covers Object- Oriented Programming with C++, focusing on classes, objects, functions, arrays, and strings, enabling students to develop structured and modular software applications. Practical exposure to shell scripting and C++ programming strengthens problem-solving and application development skills.

Course Objective:

- To understand the Linux operating system, its file system, commands, utilities, and memory management policies.
- To develop skills in shell scripting for process automation, text processing, and system administration tasks.
- To learn the principles of Object-Oriented Programming (OOP) using C++, including classes, objects, constructors, functions, and data encapsulation.
- To gain practical experience in implementing OOP concepts for software development using C++ arrays, strings, and class structures.

Course Outcomes:

- Apply Linux commands and shell scripting for file handling, automation, and system utilities.
- Develop shell and AWK scripts for text processing, data manipulation, and computations.
- Implement UNIX system calls in C for file, directory, and process management.
- Demonstrate process creation, client- server communication, and inter-process interaction in C.

UNIT- I

Linux Basics: Introduction to Linux, File System of the Linux, General usage of Linux kernel 7 basic commands, Linux users and group, Permissions for file, directory and users, Searching a file & directory, Zipping and unzipping concepts, Editors and Utilities. Memory Management Policies: Swapping – Demand paging.

Unit-II:

Linux Utilities-File handling utilities, Security by file permissions, Process utilities, Disk utilities, Networking commands, Filters, Text processing utilities and Backup utilities. Sed-Scripts, Operation, Addresses, Commands, awk-Execution, Fields and Records, Scripts, Operation, Patterns, Actions, Associative Arrays, String and Mathematical functions, System commands in awk, Applications.

Unit-III:

Shell programming with Bourne again shell(bash)- Introduction, shell responsibilities, pipes and Redirection, here documents, running a shell script, the shell as a programming language, shell

meta characters, file name substitution, shell variables, command substitution, shell commands, the environment, quoting, test command, control structures, arithmetic in shell, shell script examples, interrupt processing, functions, debugging shell scripts.

Unit-IV:

Introduction to Object Oriented Programming: Need for Object Oriented Programming - Characteristics of Object-Oriented Languages – Comparison of C and C++ - Structures: Structures - Enumerations – Functions: Simple Functions – Passing Arguments to Functions – Returning Values from Functions – Reference Arguments - Overloaded Functions – Recursion – Inline Functions – Default Arguments –Scope and Storage Class – Returning by Reference – const Function Arguments.

Unit-V:

Objects and Classes: A Simple Class – C++ Objects as Physical Objects – C++ Objects as Data Types - Constructors – Objects as Function Arguments - Copy Constructor – Structures and Classes – Classes, Objects and Memory - Static class data – Constant Member functions and constant objects - Arrays and Strings: Array Fundamentals – Arrays as Class Member Data – Array of Objects – C-Strings – The Standard C++ String Class.

Text Books:

1. Unix System Programming using C++, T. Chan, PHI, 2015
2. Robert Lafore, Object Oriented Programming in C++, Fourth Edition, Tech Media, 2002. ISBN 0- 672-32308-7

Reference Books:

1. Beginning Linux Programming, 4th Edition, N. Mathew, R. Stones, Wrox, Wiley India Edition, 2007.
2. Unix Concepts and Applications, 4th Edition, Sumitabha Das, TMH, 2017.

e Resources:

NOC: Linux Programming and OOPS https://nptel.ac.in/courses/117106113

DIGITAL CMOS CIRCUIT DESIGN LAB

Course Overview: The Digital CMOS Circuit Design Lab provides hands-on experience with CMOS digital circuit design using industry-standard software tools like Mentor Graphics, Cadence, or Synopsys. Students will design, analyze, and verify various logic circuits, including multiplexers, flip-flops, counters, and memory cells, while learning physical verification and layout extraction techniques.

Course Objective:

- To apply VLSI design methodologies using standard industry EDA tools.
- To design and analyze CMOS logic circuits for digital applications.
- To perform layout extraction and physical verification for CMOS designs.
- To analyze digital CMOS circuits including sequential and combinational components.

Course Outcomes:

- Apply VLSI Design Methodologies using industry-standard tools like Mentor Graphics.
- Analyze and design basic CMOS logic circuits for full-custom IC design.
- Perform physical verification and layout extraction for CMOS circuits.
- Analyze CMOS digital circuits, including sequential and combinational logic components

List of Experiments:

Exp No.	Experiment Name
1	Inverter Characteristics.
2	NAND and NOR Gate.
3	XOR and XNOR Gate.
4	2:1 Multiplexer.
5	Full Adder.
6	RS-Latch.
7	Clock Divider.
8	JK-Flip Flop.
9	Synchronous Counter.
10	Asynchronous Counter.
11	Static RAM Cell.
12	Dynamic Logic Circuits.
13	Linear Feedback Shift Register.

Lab Requirements:

Software:

Industry Standard Software (Mentor Graphics Tool/Cadence/ Synopsys/Equivalent)

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

REAL TIME OPERATING SYSTEMS LAB

Course Objective:

The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits and ARM- Cortex.

Course Outcomes:

Demonstrate the ability to create and manage tasks, handle interrupts, and implement synchronization techniques using PERFECT RTOS on ARM-926

Implement resource allocation and synchronization mechanisms.

Interface peripheral devices (e.g., display, ADC/DAC) with the ARM-Cortex processor.

Develop embedded applications involving serial communication for data logging and modem functionality using ARM-based development boards.

List of Experiments:

Part-I: Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.

Part-II: Experiments on ARM-CORTEX processor using any open source RTOS. (Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communication with PC.
4. Implement the developer board as a modem for data communication using serial port communication between two PC's.

Lab Requirements:

Software:

- Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO- COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.

LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

Hardware:

- The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.
- Serial Cables, Network Cables and recommended power supply for the board.